

```
graph TD; CPU[Central Processing Unit 102] --- Micro[Micro code 104]; CPU --- CR[Control Register 110]; CR --- RQ[Request Queue 112]; CR --- BNRSM[Block Next Request State Machine 108]; RQ --- RSM[Request State Machine 114]; BNRSM --- BC[Bus Controller 106]; BNRSM --- AC[Arbitration Component 116];
```

Central Processing Unit  
102

Micro code  
104

Control Register  
110

Request Queue  
112

Block Next Request State Machine  
108

Request State Machine  
114

Bus Controller  
106

Arbitration Component  
116

Figure 1

FIG. 2

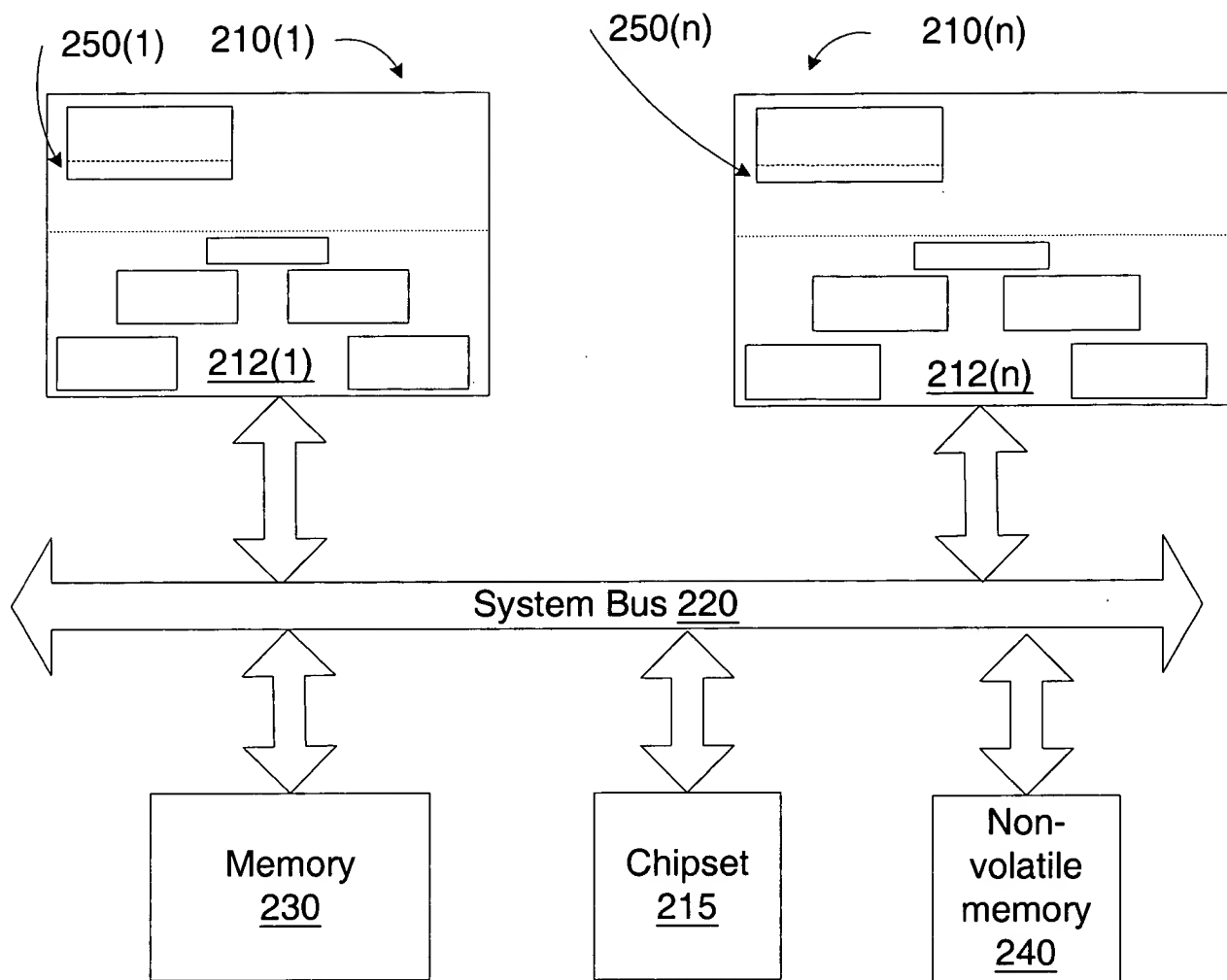


Figure 2

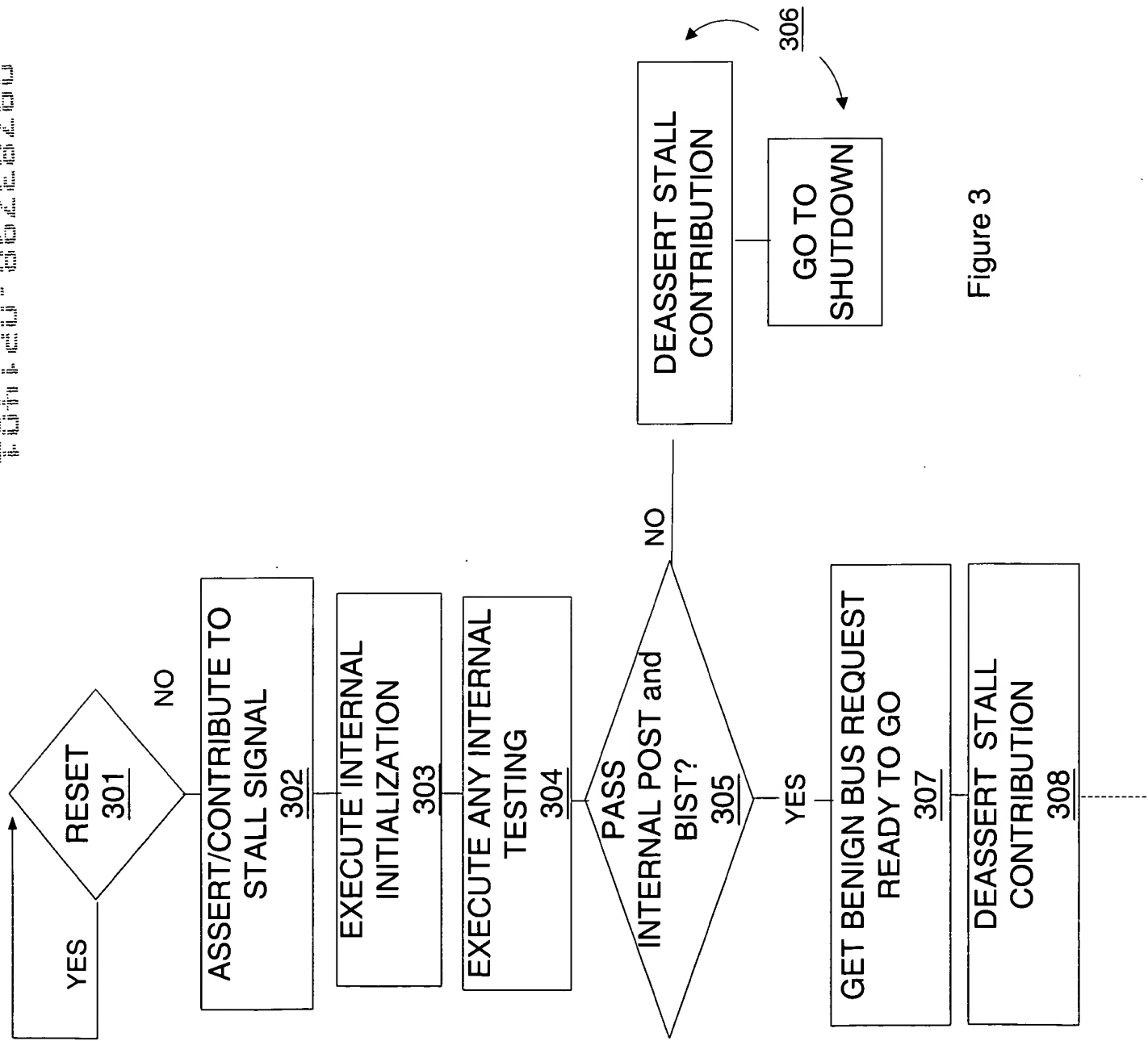


Figure 3

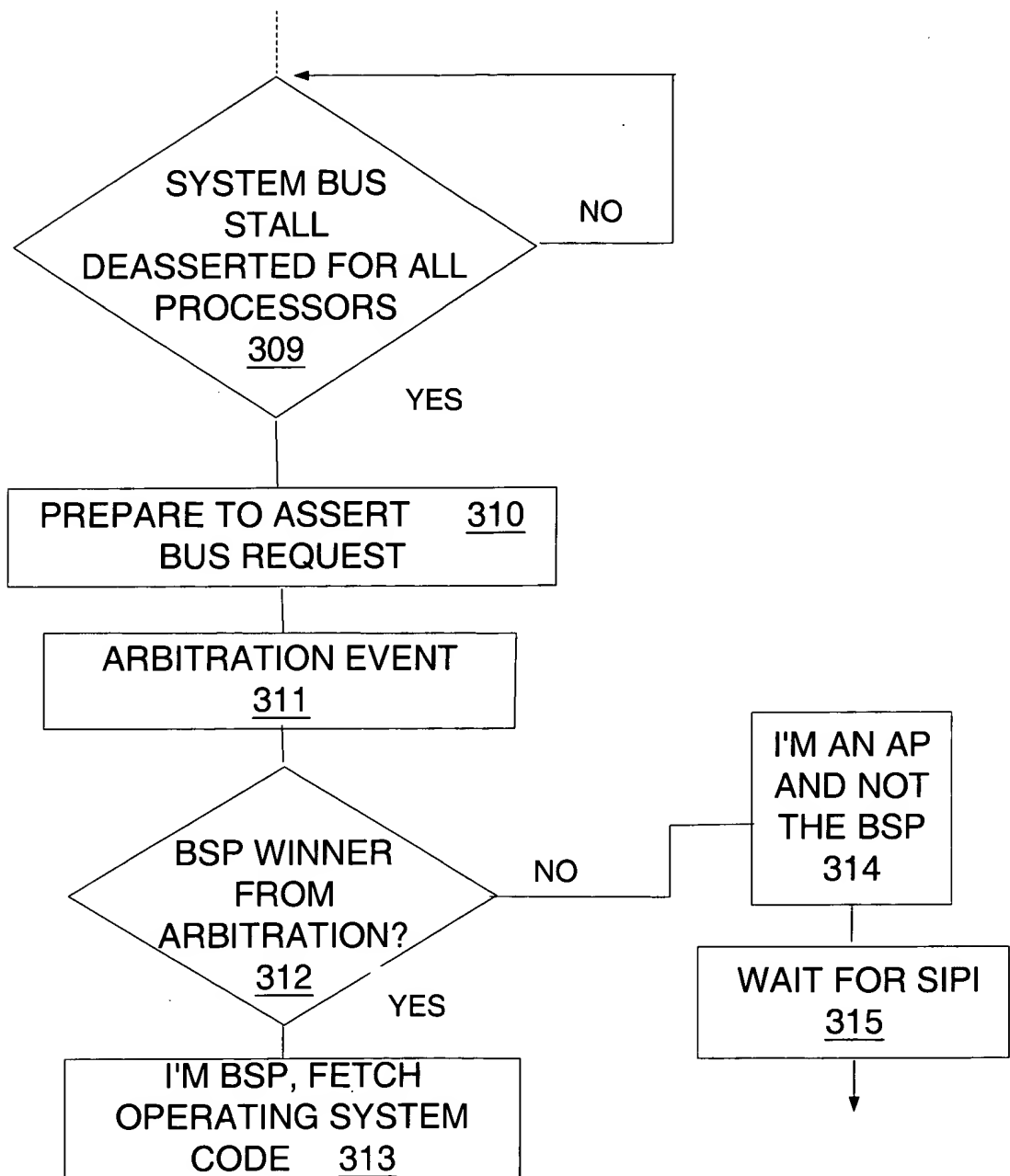


Figure 4